74HC161

Presettable synchronous 4-bit binary counter; asynchronous reset

Rev. 5 — 16 March 2021 Product data sheet

1. General description

The 74HC161 is a synchronous presettable binary counter with an internal look-head carry. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs (Q0 to Q3) of the counters may be preset HIGH or LOW. A LOW at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D0 to D3) to be loaded into the counter on the positive-going edge of the clock. Preset takes place regardless of the levels at count enable inputs (CEP and CET). A LOW at the master reset input ($\overline{MR}$) sets Q0 to Q3 LOW regardless of the levels at input pins CP, $\overline{PE}$, CET and CEP (thus providing an asynchronous clear function). The look-ahead carry simplifies serial cascading of the counters. Both CEP and CET must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH output of Q0. This pulse can be used to enable the next cascaded stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{t_{P(max)}(\text{CP to TC}) + t_{SU}(\text{CEP to CP})}$$

Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- CMOS input levels
- Synchronous counting and loading
- 2 count enable inputs for n-bit cascading
- Asynchronous reset
- Positive-edge triggered clock
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

nexperia

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC161D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC161PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

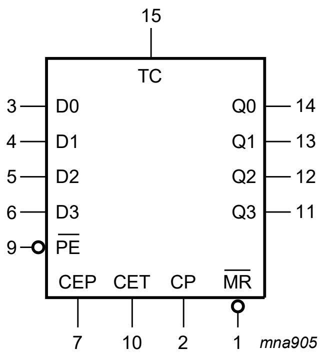


Fig. 1. Logic symbol

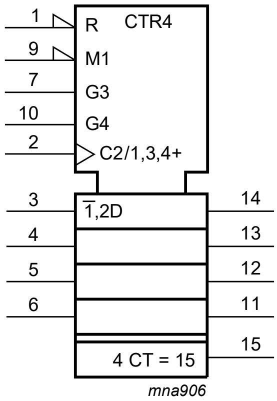


Fig. 2. IEC logic symbol

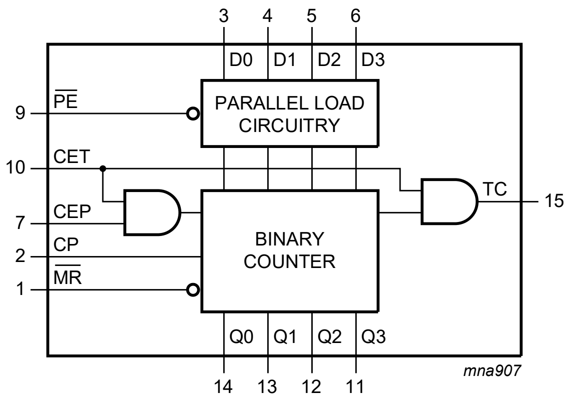


Fig. 3. Functional diagram

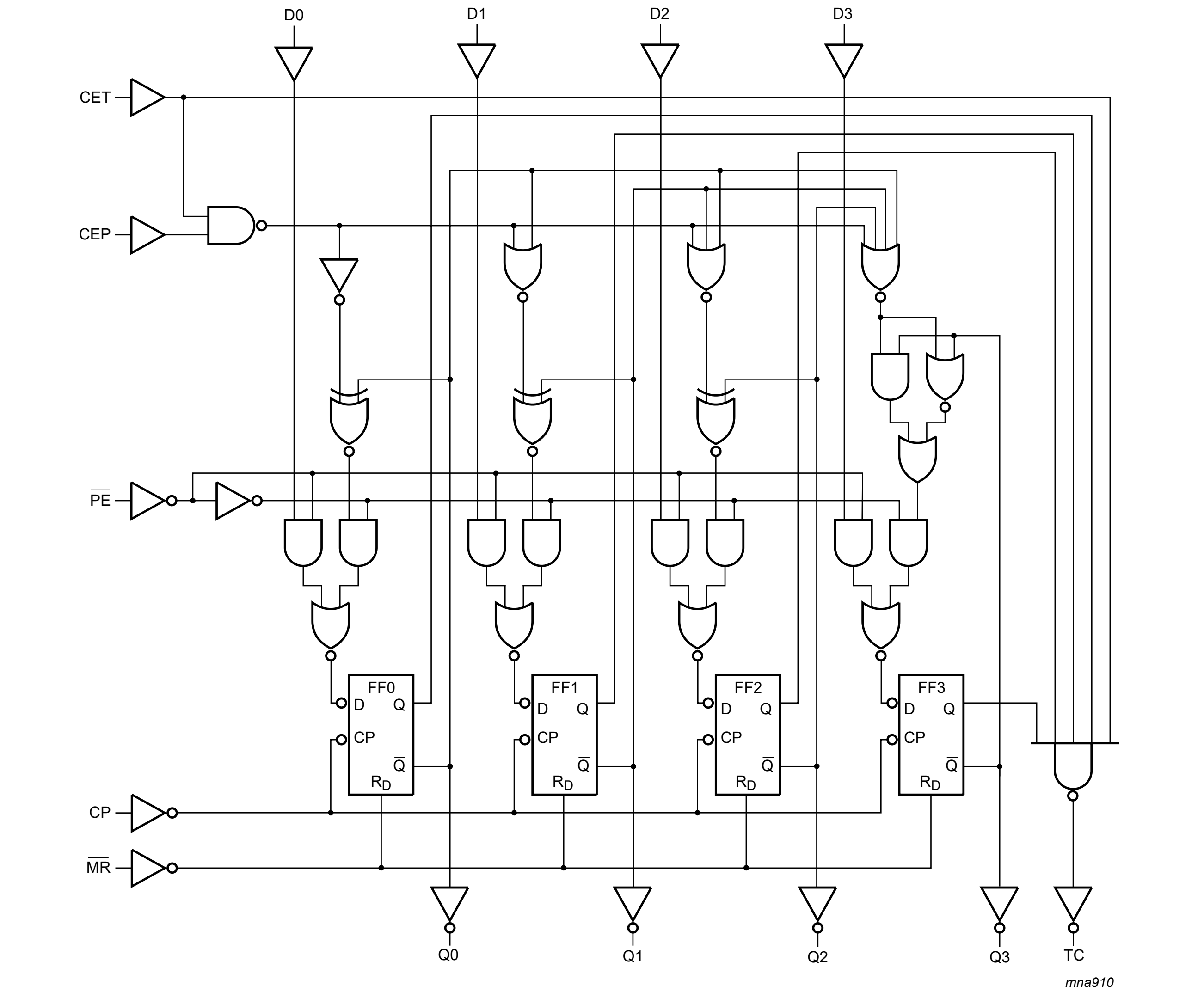


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning

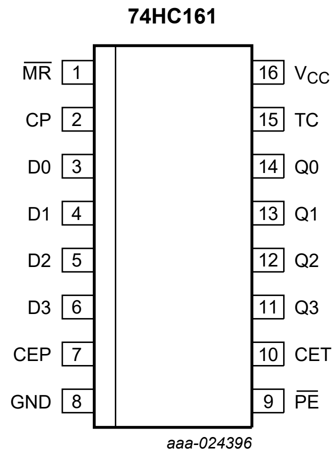


Fig. 5. Pin configuration SOT109-1 (SO16)

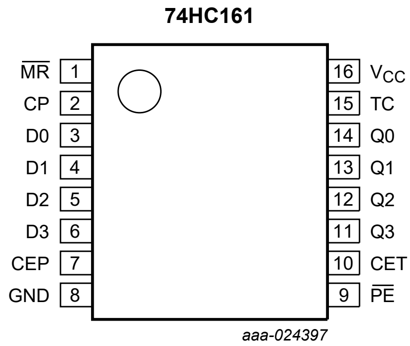


Fig. 6. Pin configuration SOT403-1 (TSSOP16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{MR}$	1	asynchronous master reset (active LOW)
CP	2	clock input (LOW-to-HIGH, edge-triggered)
D0, D1, D2, D3	3, 4, 5, 6	data input
CEP	7	count enable input
GND	8	ground (0 V)
$\overline{PE}$	9	parallel enable input (active LOW)
CET	10	count enable carry input
Q0, Q1, Q2, Q3	14, 13, 12, 11	flip-flop output
TC	15	terminal count output
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
q_n = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;
X = don't care; ↑ = LOW-to-HIGH clock transition.

Operating modes	Input						Output	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	[1]
Count	H	↑	h	h	h	X	count	[1]
Hold (do nothing)	H	X	l	X	h	X	q_n	[1]
	H	X	X	l	h	X	q_n	L

[1] The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH)

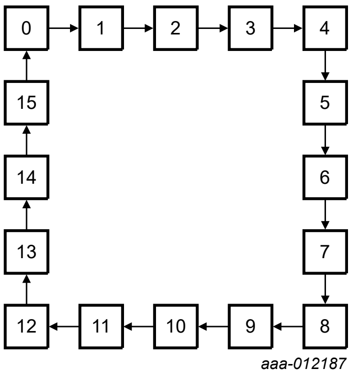
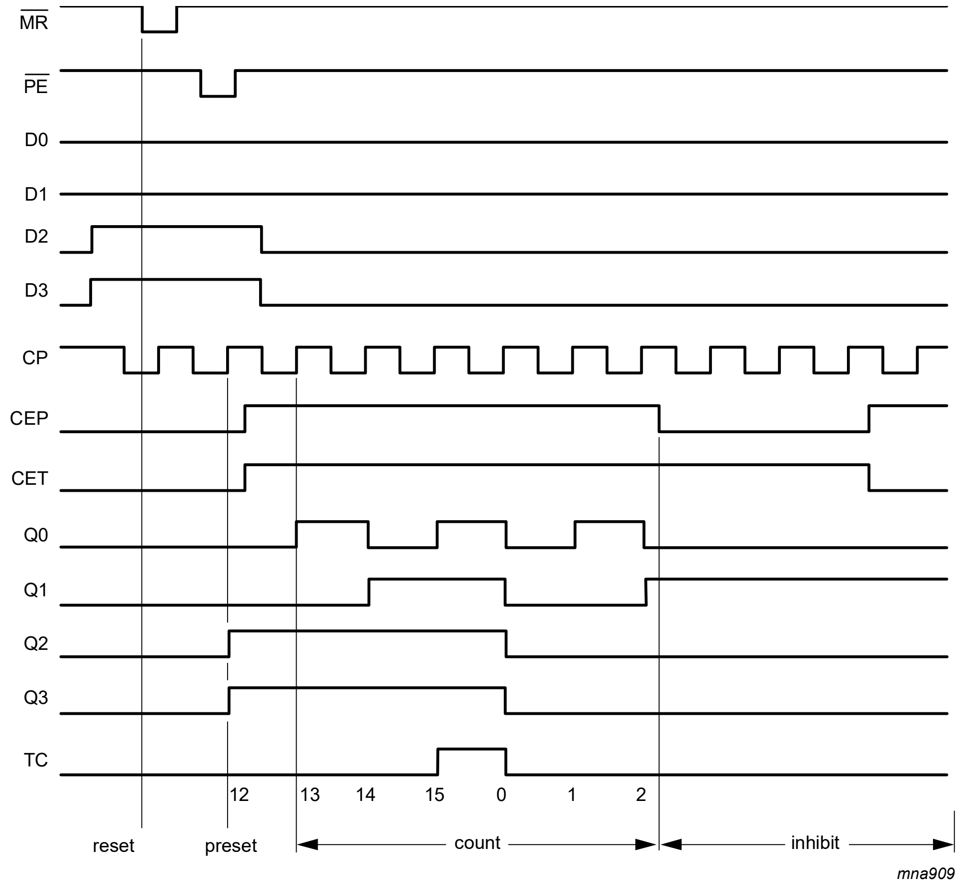


Fig. 7. State diagram



Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit.

Fig. 8. Typical timing sequence

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V	-	±20	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V	-	±20	mA
I_O	output current	V_O = -0.5 V to V_{CC} + 0.5 V	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	[1]	-	500	mW

[1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	ns/V
		V_{CC} = 4.5 V	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = -20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80.0	-	160.0	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

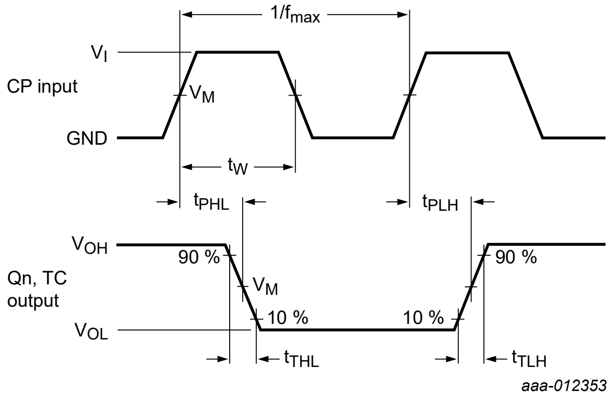
Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Fig. 14.

Symbol	Parameter	Conditions		25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	CP to Qn; see Fig. 9 [1]								
		V_{CC} = 2.0 V	-	61	190	-	240	-	285	ns
		V_{CC} = 4.5 V	-	22	38	-	48	-	57	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	19	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	18	32	-	41	-	48	ns
		CP to TC; see Fig. 9								
		V_{CC} = 2.0 V	-	69	215	-	270	-	325	ns
		V_{CC} = 4.5 V	-	25	43	-	54	-	65	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	21	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	20	37	-	46	-	55	ns
		CET to TC; see Fig. 10								
		V_{CC} = 2.0 V	-	33	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	12	30	-	38	-	45	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	10	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	10	26	-	38	-	31	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see Fig. 11								
		V_{CC} = 2.0 V	-	63	210	-	265	-	315	ns
		V_{CC} = 4.5 V	-	23	42	-	53	-	63	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	20	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	18	36	-	45	-	54	ns
		$\overline{MR}$ to TC; see Fig. 11								
		V_{CC} = 2.0 V	-	63	220	-	275	-	330	ns
		V_{CC} = 4.5 V	-	23	44	-	55	-	66	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	20	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	18	37	-	47	-	56	ns
t_t	transition time	see Fig. 9 and Fig. 10 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	CP; HIGH or LOW; see Fig. 9								
		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
		$\overline{MR}$; LOW; see Fig. 11								
		V_{CC} = 2.0 V	80	19	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{rec}	recovery time	$\overline{MR}$ to CP; see Fig. 11								
		V_{CC} = 2.0 V	100	19	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	7	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	6	-	21	-	26	-	ns
t_{su}	set-up time	Dn to CP; see Fig. 12								
		V_{CC} = 2.0 V	80	25	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	9	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	7	-	17	-	20	-	ns
		$\overline{PE}$ to CP; see Fig. 12								
		V_{CC} = 2.0 V	100	30	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	11	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	9	-	21	-	26	-	ns
		CEP, CET to CP; see Fig. 13								
		V_{CC} = 2.0 V	170	47	-	215	-	255	-	ns
		V_{CC} = 4.5 V	34	17	-	43	-	51	-	ns
		V_{CC} = 6.0 V	29	14	-	37	-	43	-	ns
t_h	hold time	Dn, $\overline{PE}$, CEP, CET to CP; see Fig. 12 and Fig. 13								
		V_{CC} = 2.0 V	0	-14	-	0	-	0	-	ns
		V_{CC} = 4.5 V	0	-5	-	0	-	0	-	ns
		V_{CC} = 6.0 V	0	-4	-	0	-	0	-	ns
f_{max}	maximum frequency	CP; see Fig. 9								
		V_{CC} = 2.0 V	4.6	13	-	3.6	-	3.0	-	MHz
		V_{CC} = 4.5 V	23	40	-	18	-	15	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	44	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	27	48	-	21	-	18	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 5 V; f_i = 1 MHz [3]	-	33	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \sum(C_L \times V_{CC}{}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}{}^2 \times f_o)$ = sum of outputs.

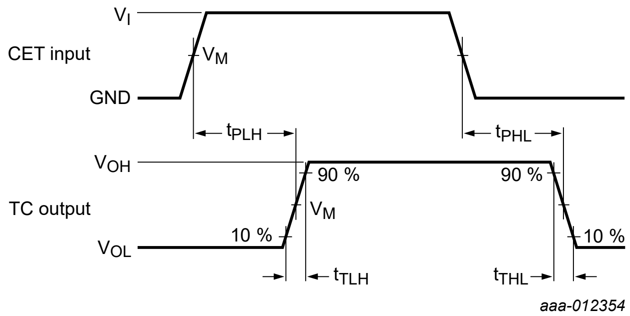
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

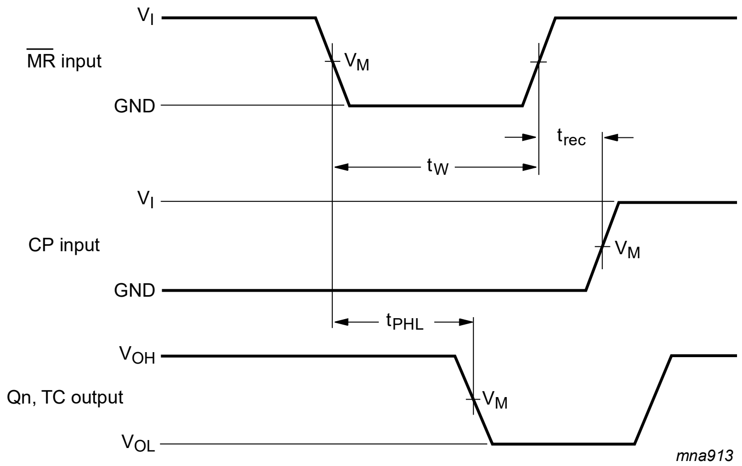
Fig. 9. The clock (CP) to outputs (Qn, TC) propagation delays, pulse width, output transition times and maximum frequency



Measurement points are given in Table 8.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

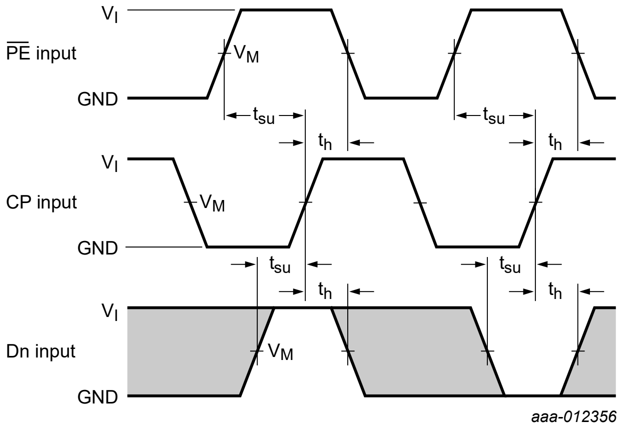
Fig. 10. The count enable carry input (CET) to terminal count output (TC) propagation delays and output transition times



Measurement points are given in Table 8.

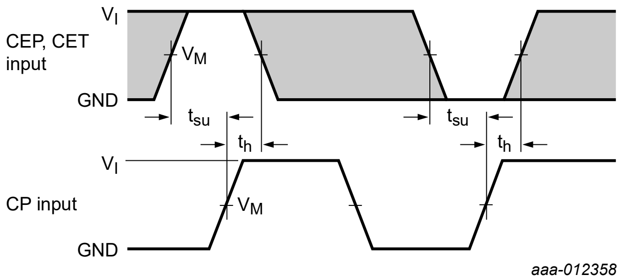
Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 11. The master reset ($\overline{MR}$) pulse width, master reset to output (Qn, TC) propagation delays, and the master reset to clock (CP) recovery times



Measurement points are given in Table 8.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 12. The data input (Dn) and parallel enable input ($\overline{PE}$) set-up and hold times

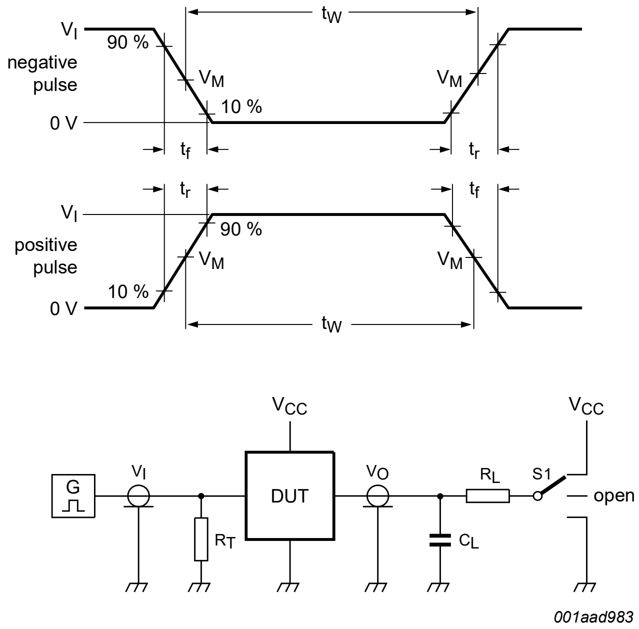


Measurement points are given in Table 8.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 13. The count enable input (CEP) and count enable carry input (CET) set-up and hold times

Table 8. Measurement points

Input		Output
V_M	V_I	V_M
0.5 × V_{CC}	GND to V_{CC}	0.5 × V_{CC}



Test data is given in Table 9.
Test circuit definitions:
R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator
C_L = Load capacitance including jig and probe capacitance
R_L = Load resistance.
S1 = Test selection switch

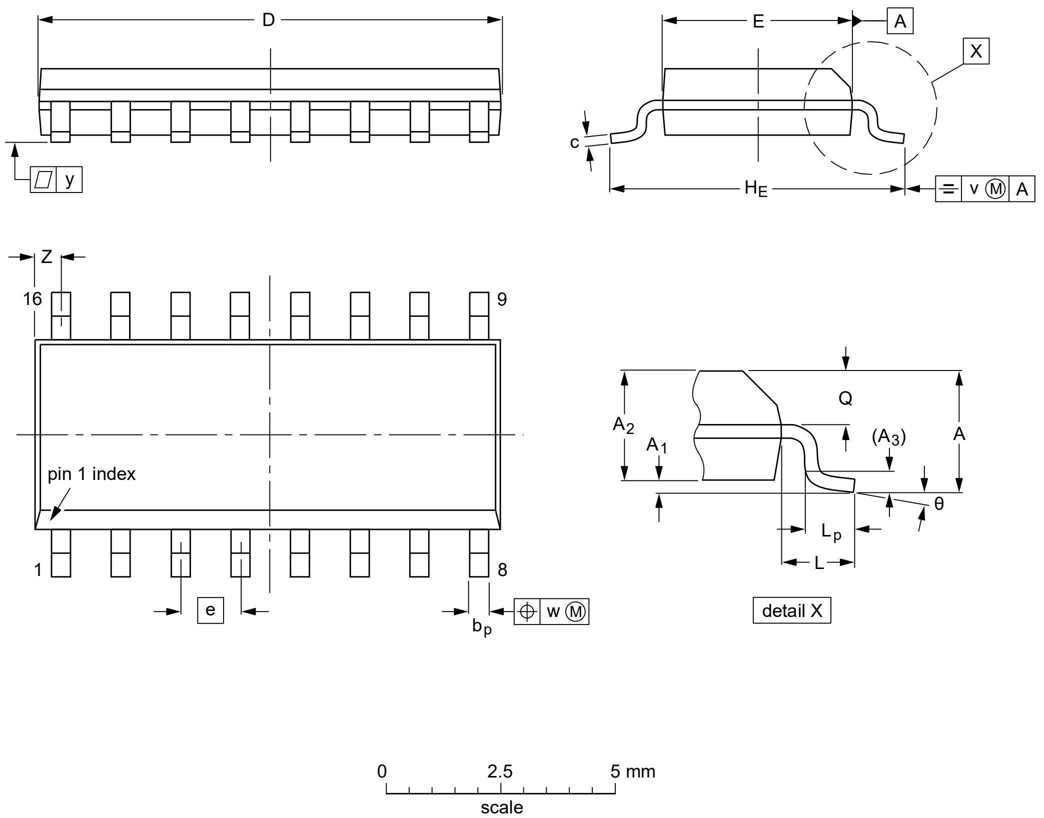
Fig. 14. Test circuit for measuring switching times

Table 9. Test data

Input		Load		S1 position
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

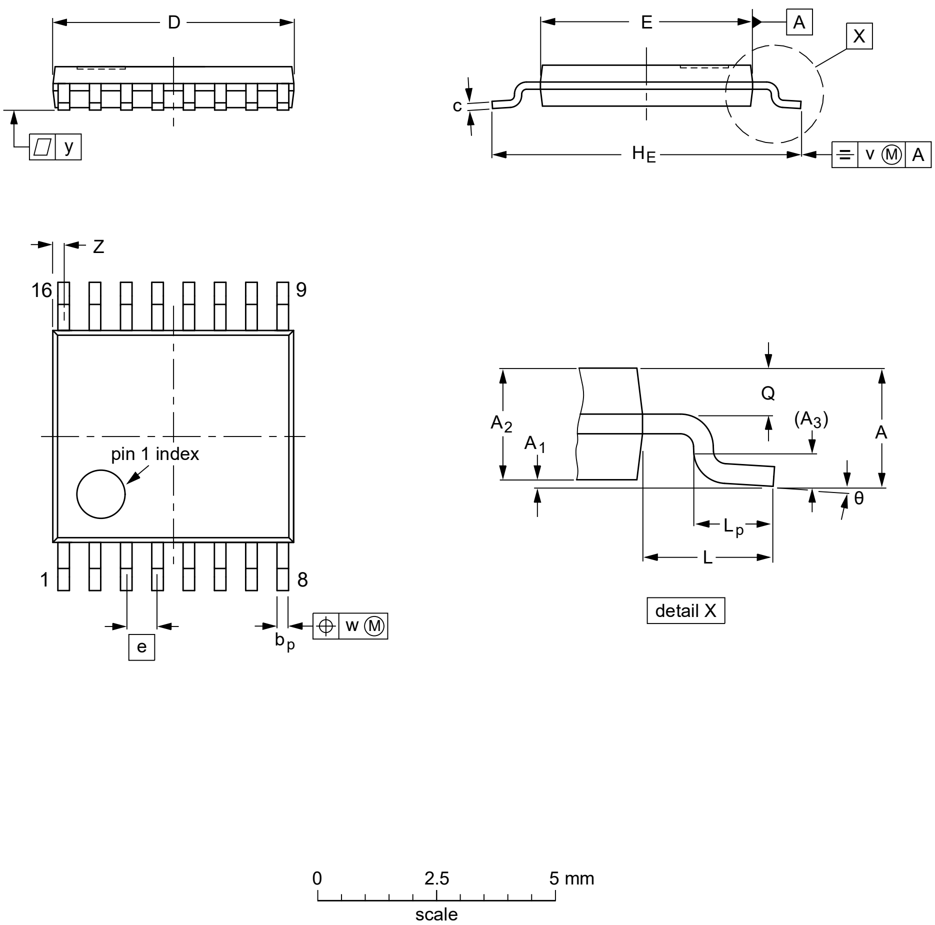
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig. 15. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^{o} 0^{o}

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 16. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC161 v.5	20210316	Product data sheet	-	74HC161 v.4
Modifications:	• Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation updated. • Type number 74HC161DB (SOT338-1 / SSOP16) removed.			
74HC161 v.4	20181004	Product data sheet	-	74HC161 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74HC161 v.3	20170104	Product data sheet	-	74HC_HCT161 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HCT161D, 74HCT161DB, 74HCT161PW removed.			
74HC_HCT161 v.2	19901201	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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